WHAT IS CLAIMED IS:

1. A magnetic random access memory comprising:

a vertical structure transistor;

a read line connected to a gate electrode formed at a sidewall of the vertical structure transistor;

a magnetic tunnel junction cell formed on a drain junction region existing over an upper portion of vertical structure; and

a write line formed on an upper portion of the magnetic tunnel junction cell.

2. The magnetic random access memory of claim 1, wherein the vertical structure transistor has a circular pillar extending perpendicularly to a semiconductor substrate.

3. The magnetic random access memory of claim 2, further comprising:

the drain junction region formed in an upper portion of the circular pillar;

a source junction region formed at a bottom portion of the circular pillar extending into the semiconductor substrate;

a channel region formed at the center of the circular pillar; and

a gate insulation layer formed at the sidewall of the circular pillar between the gate electrode and the sidewall of the circular pillar.

4. The magnetic random access memory of claim 1, wherein the read line is parallel to the write line.

5. The magnetic random access memory of claim 1, wherein the magnetic tunnel junction cell has a width equal to a width of any one of the group consisting of the vertical structure transistor, the read line, the write line, the bit line, and the circular pillar.

6. A magnetic random access memory comprising:

a vertical structure transistor;

a first word line connected to a gate electrode of the vertical structure transistor;

a contact line connected to the vertical structure transistor;

a magnetic tunnel junction cell formed on the contact line;

a bit line formed on the magnetic tunnel junction cell; and

a second word line formed on the bit line over an upper portion of the magnetic tunnel junction cell.

7. The magnetic random access memory of claim 6, wherein the vertical structure transistor includes a circular pillar, a gate oxide layer, and a gate electrode, wherein the gate oxide layer is formed at a sidewall of a substrate having a source junction region and a drain junction region.

8. The magnetic random access memory of claim 7, wherein the drain junction region is formed in an upper portion of the circular pillar, and the source junction region is formed at a bottom portion of the circular pillar extending into the substrate surface.

9. The magnetic random access memory of claim 6, wherein the circular pillar is more than 0.5 μm in height.

10. The magnetic random access memory of claim 6, wherein the magnetic tunnel junction cell is a stacked structure including a semi-magnetic layer, a pinned ferromagnetic layer, a tunnel junction layer, and a free ferromagnetic layer.

11. The magnetic random access memory of claim 6, wherein the magnetic tunnel junction cell has a planar area equal to the area of an intersection of the bit line and the second word line.

12. The magnetic random access memory of claim 6, wherein the bit line is perpendicular to the first word line, and wherein the second word line is perpendicular to the bit line and is parallel to the first word line.

13. A method for forming the magnetic random access memory comprising the steps of:

etching a semiconductor substrate by photolithography using an active mask to form a circular pillar, the semiconductor having a top surface;

forming a gate oxide layer on the entire top surface of the semiconductor substrate;

performing ion implantation of a high concentration impurity on the substrate and on a top portion of the circular pillar by a drive-in process, thereby forming a drain junction region on the upper side of the circular pillar and a source junction region on the bottom of the circular pillar extending into the substrate surface;

forming a first word line of a gate electrode by forming a planarized conductor layer for the gate electrode exposing the drain junction region and then patterning the planarized conductor layer;

forming a planarized first interlayer insulation layer;

forming a contact line contacting the drain junction region through the first interlayer insulation layer;

forming a semi-magnetic layer, a pinned ferromagnetic layer, a tunnel junction layer, and a free ferromagnetic layer above the contact line;

forming a magnetic tunnel junction cell by patterning the semi-magnetic layer, the pinned ferromagnetic layer, the tunnel junction layer, and the free ferromagnetic layer by photolithography using a magnetic tunnel junction cell mask;

forming a planarized second interlayer insulation layer exposing the magnetic tunnel junction cell;

forming a bit line contacting the free ferromagnetic layer; and

forming a second word line over the magnetic tunnel junction cell and above the bit line.

14. The method of claim 13, wherein the step of performing ion implantation of the high concentration impurity is performed with an energy of more than 30 KeV and at a dose of more than 5E14 ions/cm^2.

15. The method of claim 13, wherein the second word line is parallel to and has the same width as the first word line.

16. A method for forming the magnetic random access memory comprising the steps of:

etching a semiconductor substrate by photolithography using an active mask thereby forming a circular pillar extending above a top surface of the substrate;

forming a gate oxide layer on the entire top surface of the substrate;

performing an ion implantation of a high concentration impurity and drive-in processes, thereby forming a drain junction region on an upper portion of the circular pillar and a source junction region on a bottom portion of the circular pillar and on the substrate;

forming a conductor layer for a gate electrode at a predetermined thickness on the substrate, and performing an anisotropic etching process, thereby forming a gate electrode in the form of a conductor spacer at a sidewall of the circular pillar;

forming a planarized first interlayer insulation layer;

forming a contact line contacting the drain junction region through the first interlayer insulation layer;

forming a semi-magnetic layer, a pinned ferromagnetic layer, a tunnel junction layer, and a free ferromagnetic layer above the contact line;

forming the magnetic tunnel junction cell by patterning the semi-magnetic layer, the pinned ferromagnetic layer, the tunnel junction layer, and the free ferromagnetic layer by photolithography using a magnetic tunnel junction cell mask;

forming a planarized second interlayer insulator exposing the magnetic tunnel junction cell;

forming a bit line contacting the free ferromagnetic layer; and

forming a second word line over an upper portion of the magnetic tunnel junction cell and above the bit line.

17. The method of claim 16, wherein the step of performing ion implantation of the high concentration impurity is performed with an energy of more than 30 KeV, at a dose of more than 5E14 ions/cm^2.

18. The method of claim 16, wherein the gate electrode is a first word line and wherein the steps of claim 16 are repeated to form a plurality of magnetic random access memories a plurality of first word lines, a plurality of circular pillars, and a plurality of second word lines, wherein the plurality of first word lines are spaced apart a distance that is 1.5 times larger than the distance between the plurality of circular pillars along one of said plurality of first word lines or along one of said plurality of the second word lines, by anisotropically etching the conductor layers for the plurality of first word lines without using separate masks.

19. The method of claim 17, wherein the first word line and the second word line have equal width.